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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/734,704	12/13/2000	Kenji OI	1076.1059/JDH	3349

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EXAMINER	
DANG, KHANH NMN	

ART UNIT	PAPER NUMBER
2181	3

DATE MAILED: 09/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/734,704	OI ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-31 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-31 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 11, it is unclear what may be the essential structural cooperative relationships between the "analysis circuit" (claim 2), "first analysis circuit" (claim 11), and "second analysis circuit" (claim 11).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Ikegawa.

At the outset, it is first noted that similar claims will be grouped together to avoid repetition in explanation.

As broadly drafted, these claims do not define any structure/step that differs from Ikegawa. With regard to claims 1, 2, 5, 9, and 10, Ikegawa discloses an interface (IEEE 1394 interface) having a plug and play function and connected to a host controller (101, for example), wherein the interface (IEEE1394 interface) performs a predetermined bus reset sequence (also "reset sequence" in Ikegawa) in response to a bus reset generated by the plug and play function (when a new I/O device

is added or removed from the 1394 bus) in accordance with a change in the status of an external bus, the interface (1394) comprising: an analysis circuit for analyzing data provided from the external bus during the bus reset sequence and for determining whether the bus reset sequence has been completed normally, wherein the analysis circuit provides the data to the host controller when the bus reset sequence has been completed normally. In Ikegawa, the 1394 serial bus corresponds to "Plug and Play", it automatically recognizes a device connected to the cable for the 1394 interface, thus recognizes connection status. When a device is removed from the interface, or a new device is added to the interface, the bus is automatically reset. The respective devices (nodes) connected to the 1394 interface/bus are provided with a node ID and are recognized as nodes constructing the network. The detection of change of network construction is made by detecting change of bias voltage at the connector port, or in another word, change in current characteristics since voltage and current are closely related. When adding/removing devices (nodes) or power ON/OFF, the network construction changes and it is necessary to recognize a new network construction by the host controller, the respective devices (nodes) detect the change of network construction, send a bus reset signal onto the bus, and send the necessary data to the host controller after the reset sequence is completed without error (or in another word, completed normally) so that the network is able to recognize the new network construction. When the reset signal is sent from one node, the physical layer of the respective nodes receives the bus reset signal, and at the same time, notifies the link layer of the occurrence of bus reset, and forwards the bus reset signal to the other nodes. When all the nodes have received the bus reset signal, a bus reset sequence is started. Thus, it is clear that the Bus Management (Fig. 7) or a so-called "analysis circuit" manages/analyzes the connection status data (obtained from, for example, adding/removing devices), and IDs of the respective device connected to the 1394 bus; and send the necessary data to the host controller only after the bus reset sequence is completed normally. No data transfer occurs during the bus

reset sequence. With regard to claims 3 and 4, the Bus Management (Fig. 7) or a so-called "analysis circuit" generates the bus reset/reset sequence upon detecting an abnormality (also "abnormality" in Ikegawa) of the data (connection status data obtained from, for example, adding/removing devices (nodes)) during the data analysis. With regard to claims 6-8, it is clearly inherent that the 1394 interface system of Ikegawa must have a storage means (buffers/registers) to temporarily store/analyze the ID/data during reset sequence so that the necessary data can be provided to the host controller after the reset sequence is successfully completed. With regard to claim 11, the interface system of Ikegawa further comprises a port circuit (associated with the connector port, Fig. 7) for detecting the status of the external bus and generating associated detection information; a physical layer circuit (associated with the physical layer, Fig. 7) connected to the port circuit to receive the data via the port circuit and generate a data packet; a link layer circuit (associated with the link layer, Fig. 7) connected to the physical layer circuit to determine whether the data packet is addressed to the interface system; and a buffer memory (see also discussion above regarding claims 6-8) connected to the link layer circuit to store the detection information and the data packet which are provided via the port circuit, the physical layer circuit, and the link layer circuit, wherein the bus management (Fig. 7) or a so-called "analysis circuit" connected to the port circuit (associated with the connector port, Fig. 7) to analyze the detection information, and to the physical layer circuit (associated with the physical layer, Fig. 7) to analyze the data packet provided during the bus reset sequence and to determine whether the data packet is normal (see also discussion above regarding claim 2). With regard to claim 12, since the IEEE 1394 interface of Ikegawa has to conform with the IEEE 1394 specification, it is clearly inherent that the ID/data packet of/from a respective devices (node) must be compared with a so-called "predetermined sequence information" or bits and "predetermined data packet" both typically stored in a memory so that the respective device can be recognized by the host/bus when added or removed from the 1394 bus. If the results are validated,

the so-called "analysis circuit" or bus management will provide the necessary data to the host controller after a normally completed bus reset sequence. See also discussion above regarding claim 2). With regard to claims 13-23, see at least discussion regarding claims 1-12 above. Note also that in Ikegawa, analyzing/managing the 1394 interface involving bus reset/reset sequence is a form of "self-diagnosis." With regard to claims 24-31, one using the 1394 interface system of Ikegawa would have performed the same steps set forth in claims 24-31.

U.S. Patent Nos. 6,169,725 to Gibbs et al., 6,018,816 to Tateyama, 6,298,405 to Ito et al., and 6,609,167 to Bastiani et al. are cited as relevant art.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 703-308-0211.

Khanh Dang
Primary Examiner